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FIG. 1

PRIOR ART

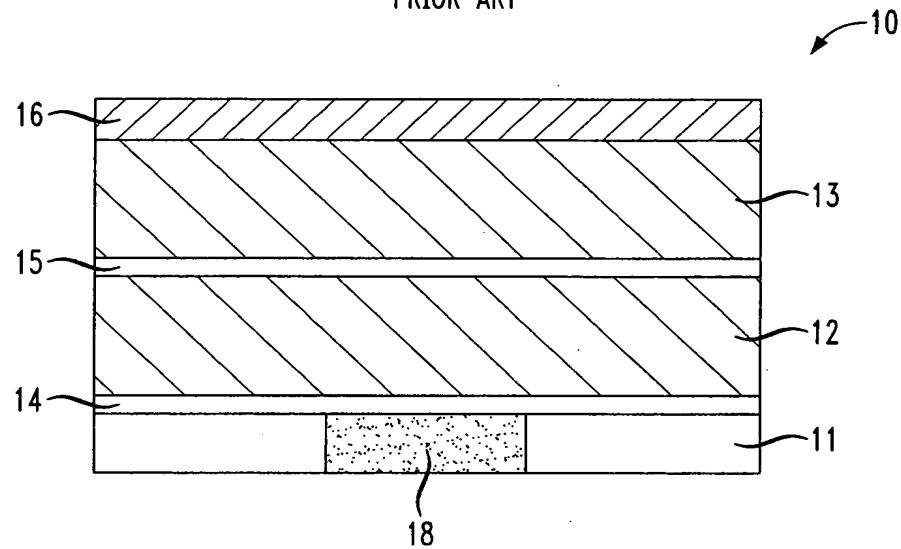
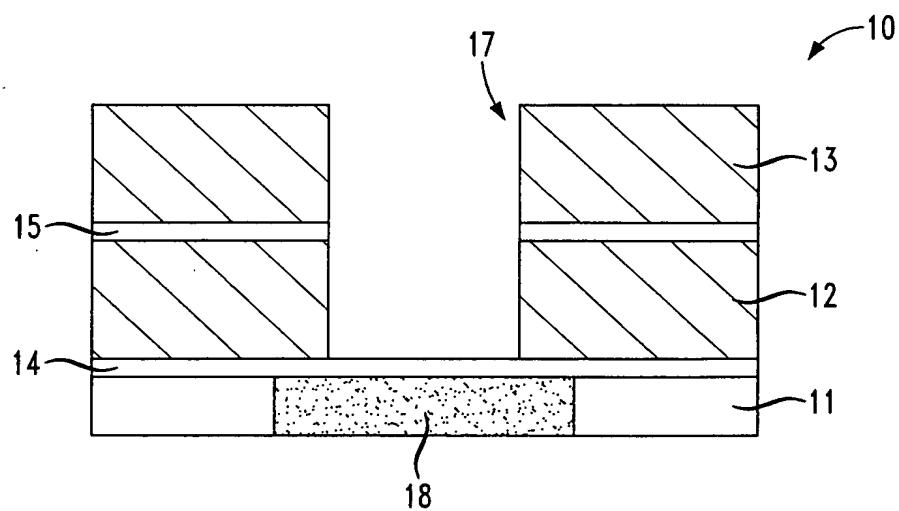
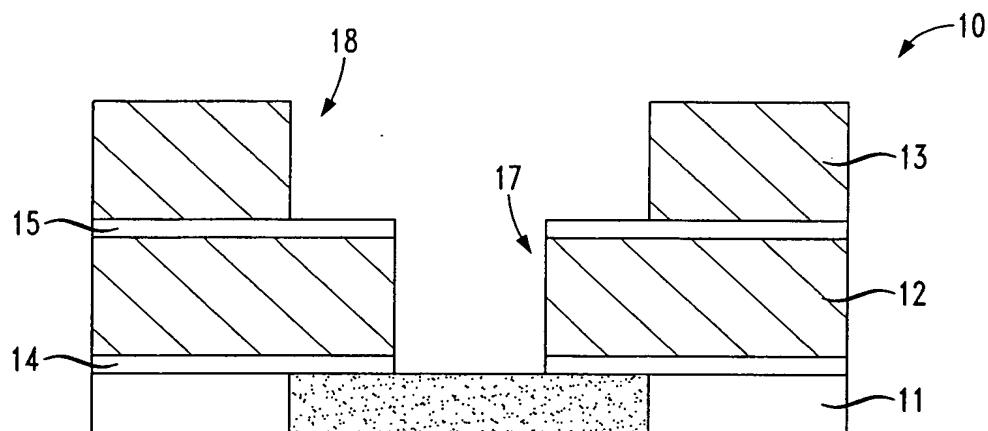
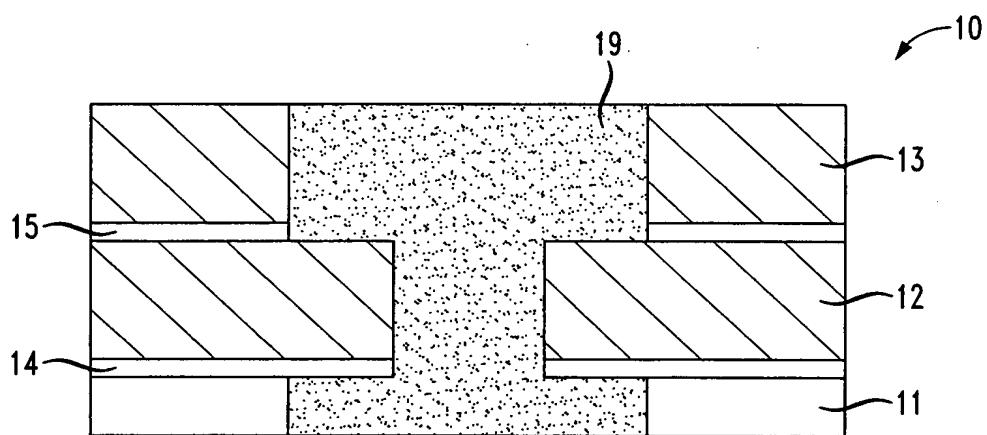


FIG. 2

PRIOR ART

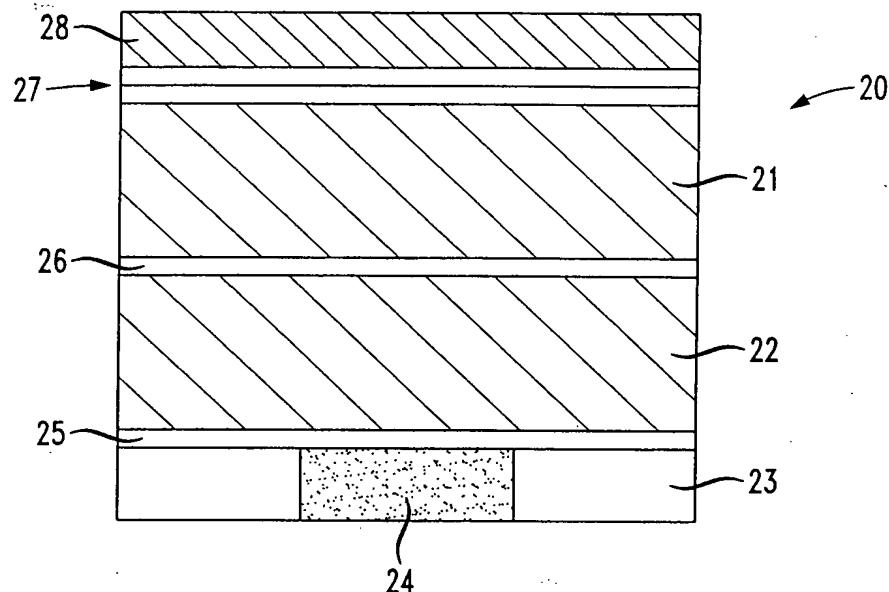


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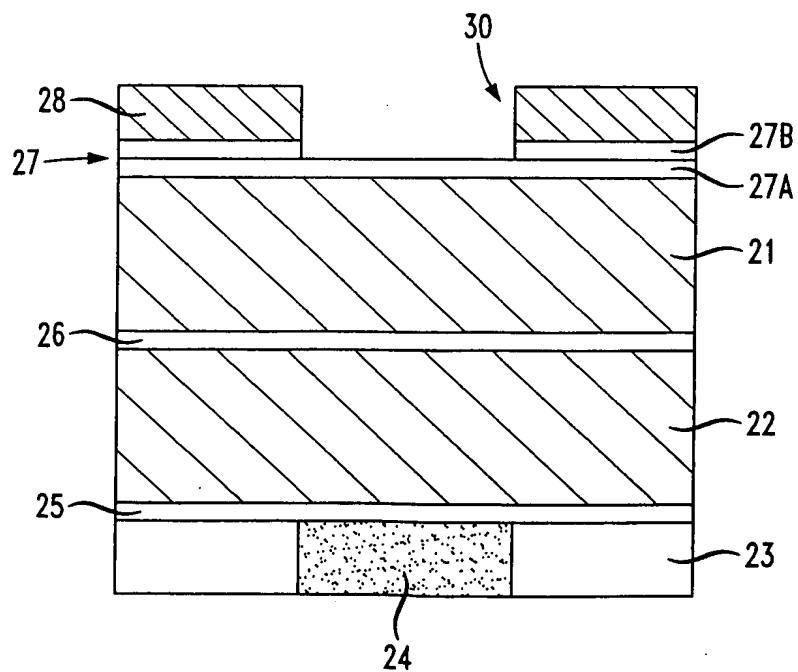
FIG. 3  
PRIOR ARTFIG. 4  
PRIOR ART

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*FIG. 5*  
PRIOR ART



*FIG. 6*  
PRIOR ART

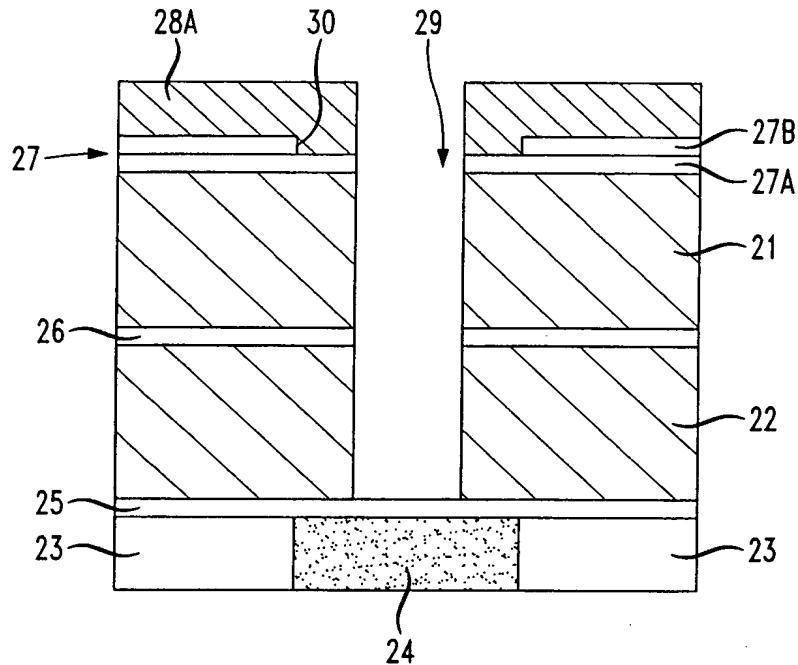


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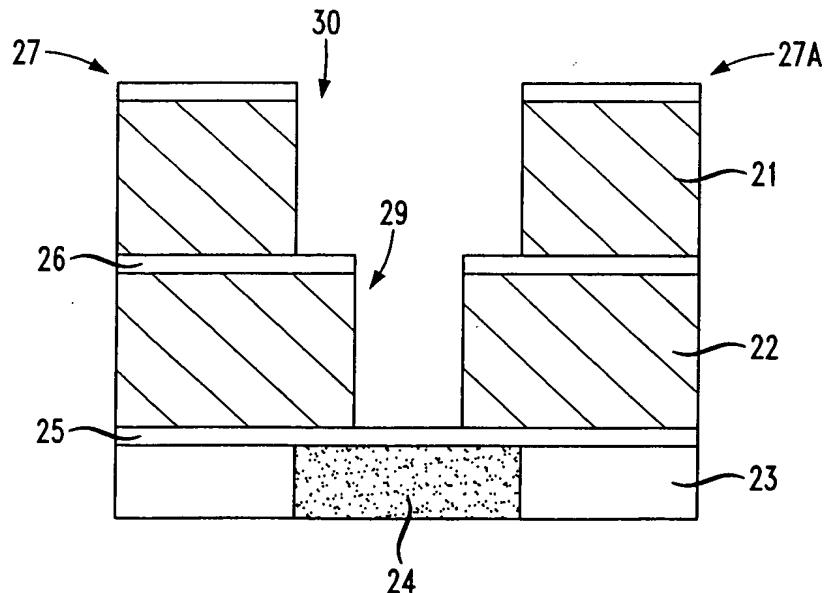
A Mask Layer and Intercept Structure for Dual Damascene Fabrication of a Semiconductor Device  
Robert L. Wolter (407-926-7700)  
Serial #10/026,257

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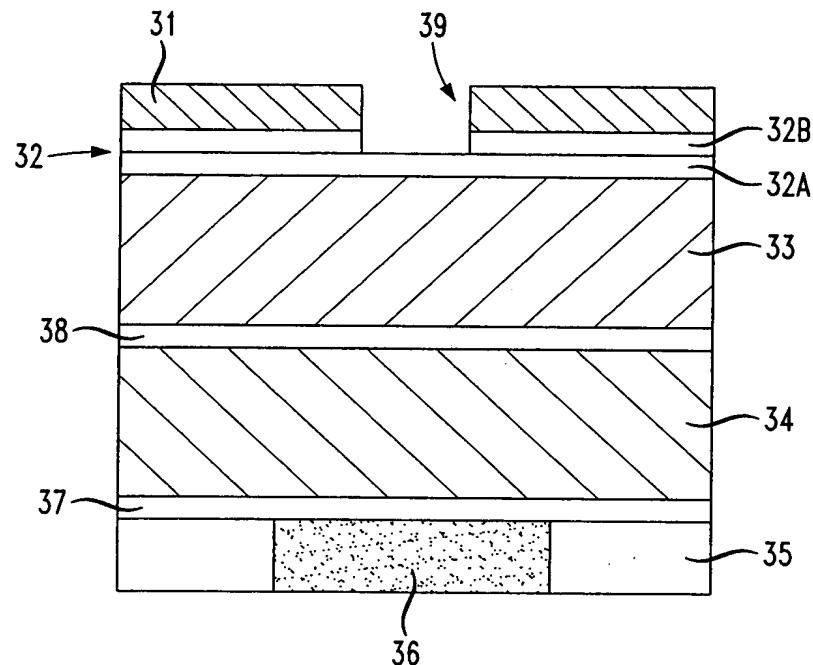
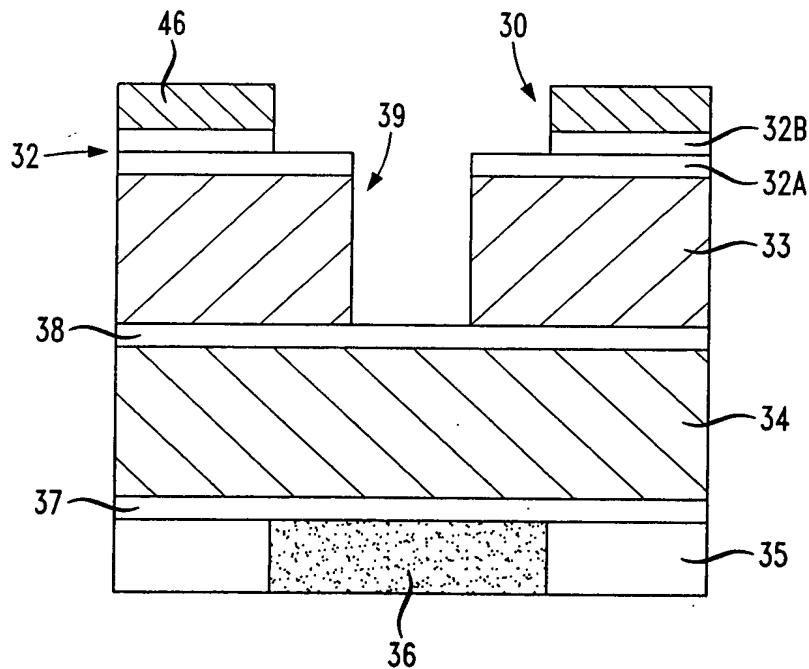
*FIG. 7*  
PRIOR ART



*FIG. 8*  
PRIOR ART



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FIG. 9  
PRIOR ARTFIG. 10  
PRIOR ART

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FIG. 11  
PRIOR ART

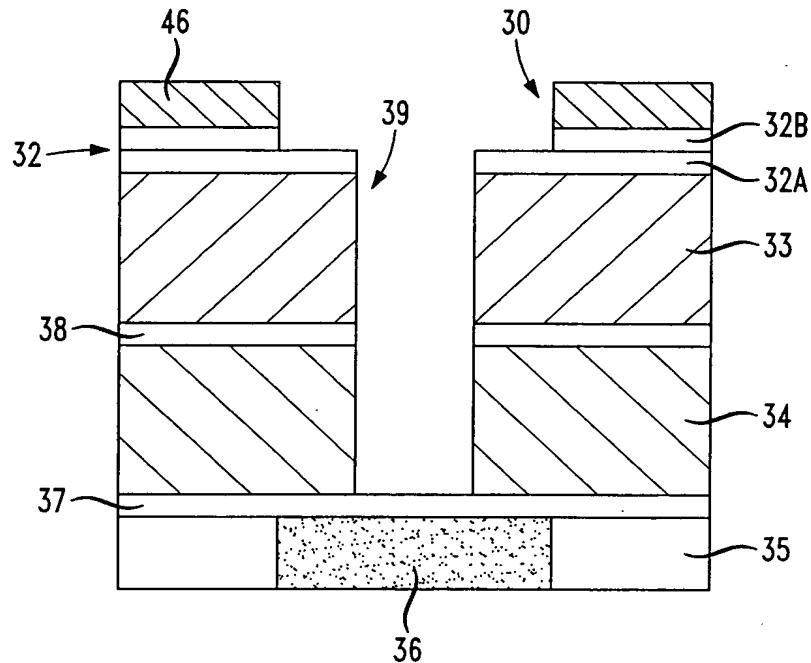
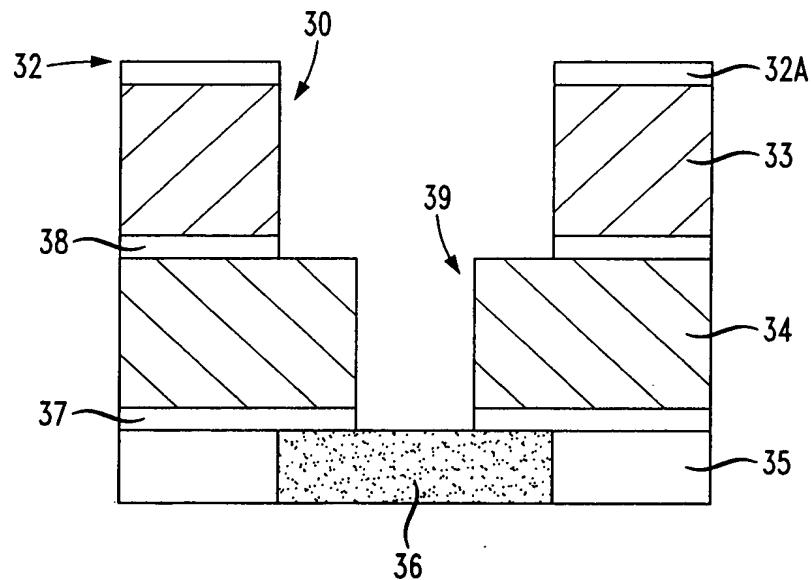
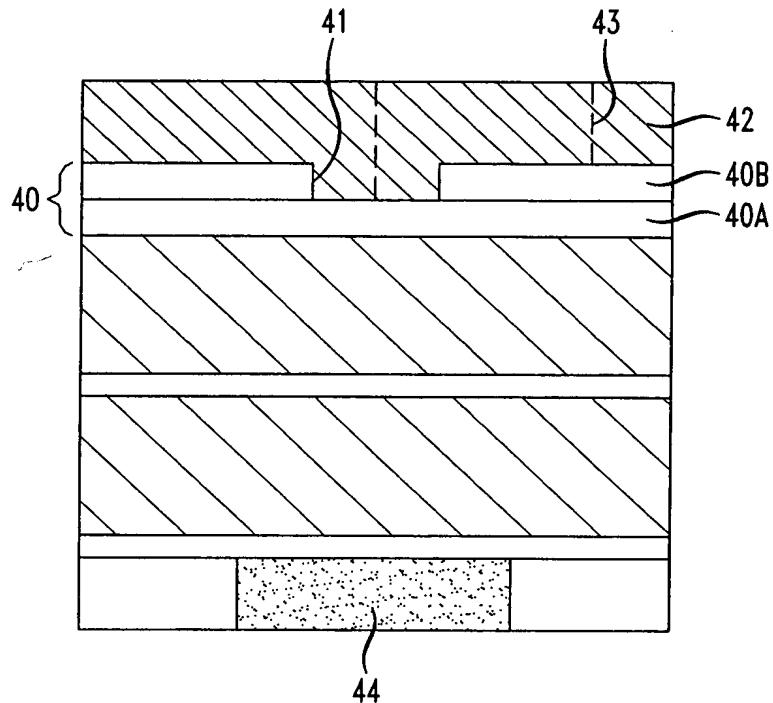


FIG. 12  
PRIOR ART

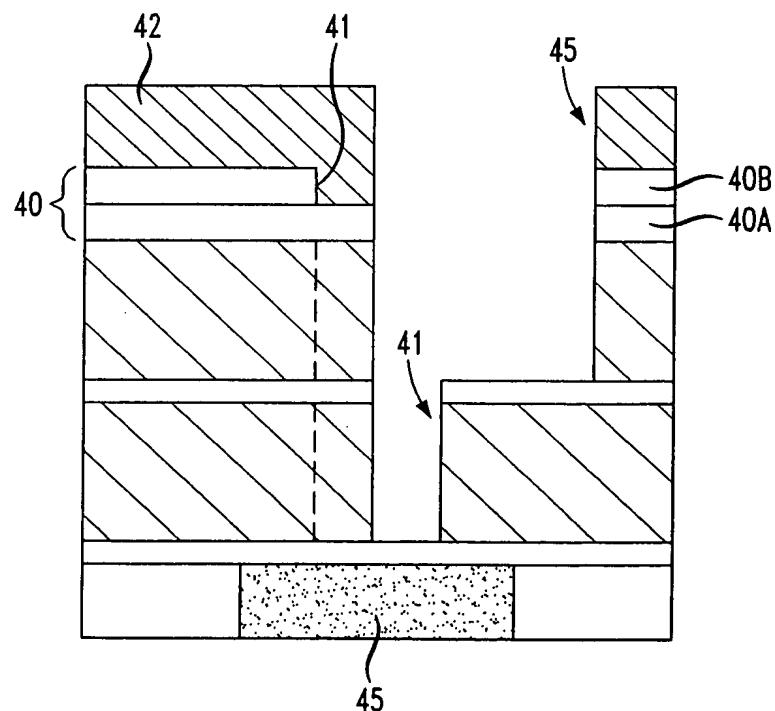


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*FIG. 13*  
PRIOR ART



*FIG. 14*  
PRIOR ART



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FIG. 15

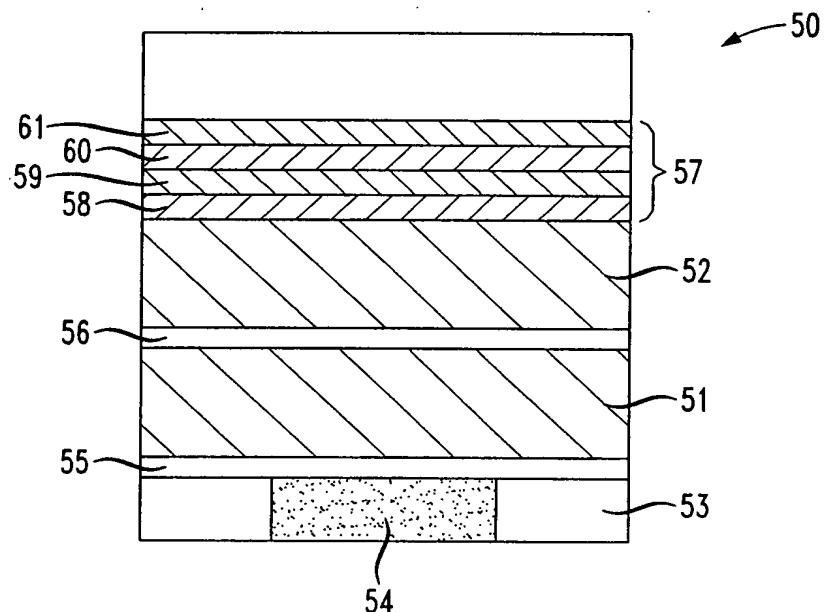
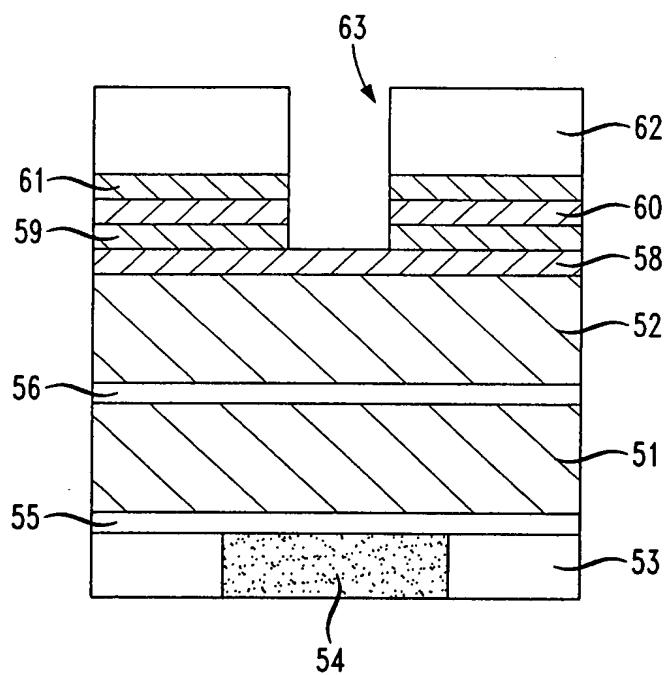


FIG. 16



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FIG. 17

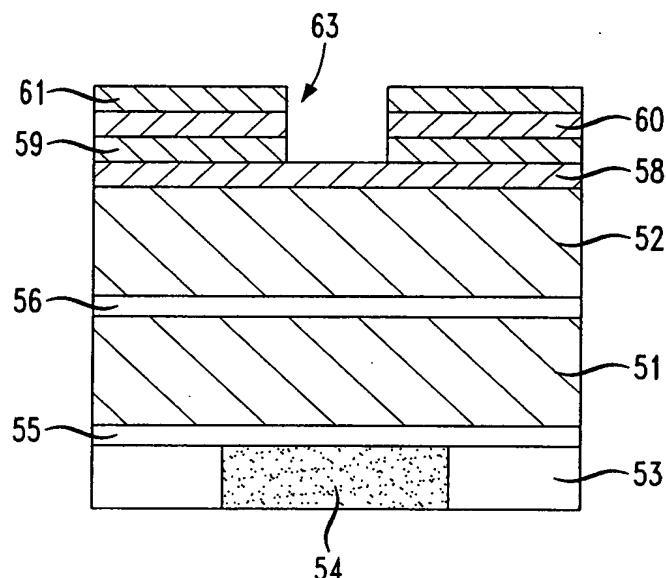
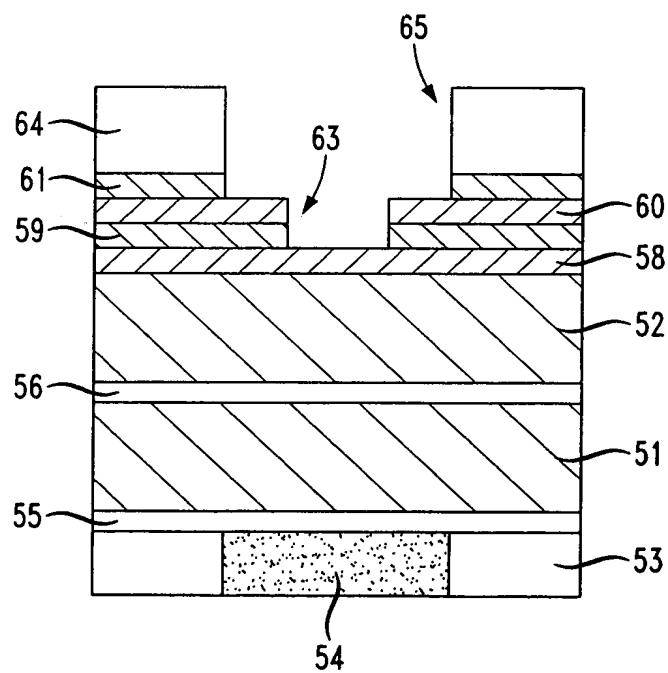


FIG. 18



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FIG. 19

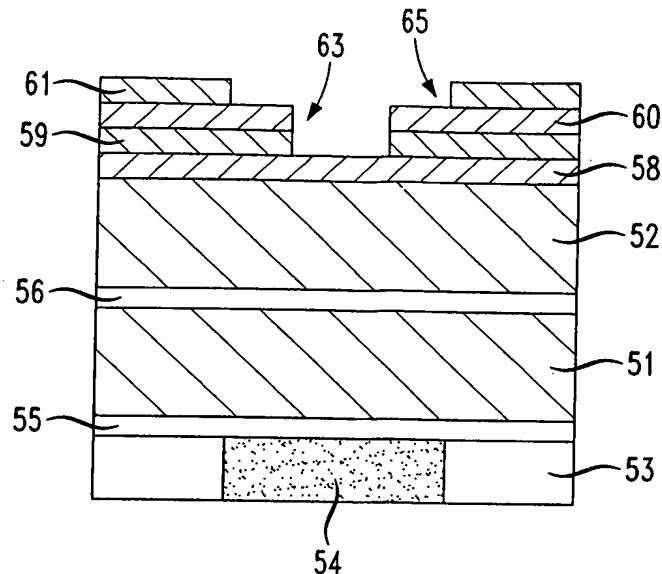
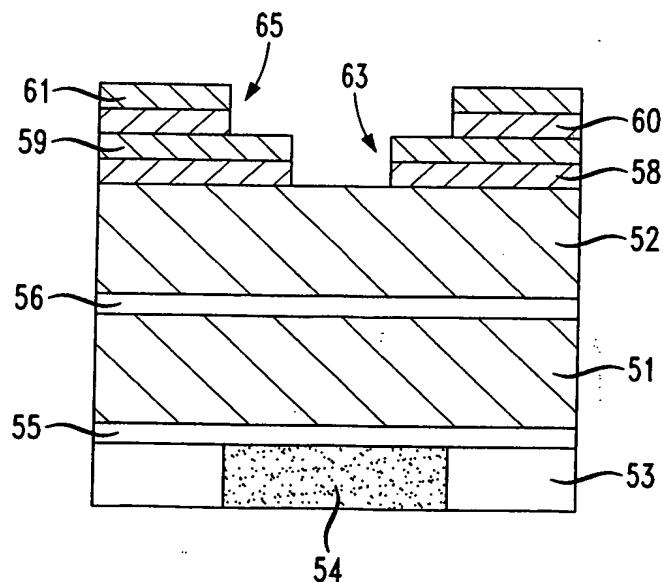


FIG. 20



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FIG. 21

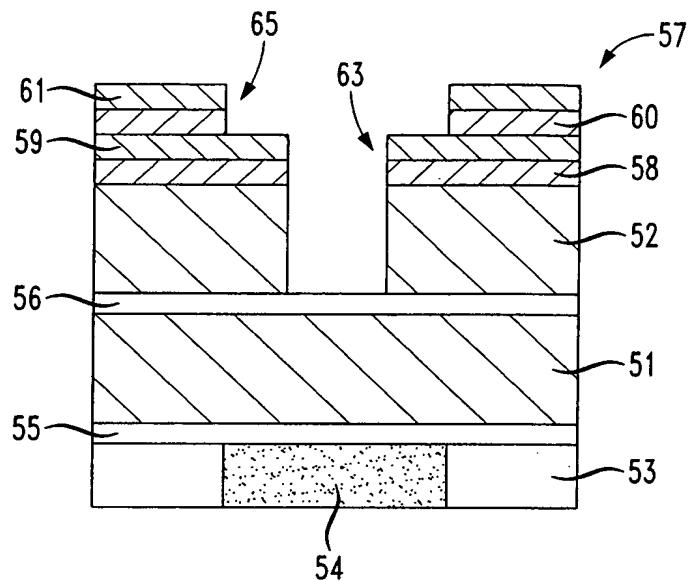
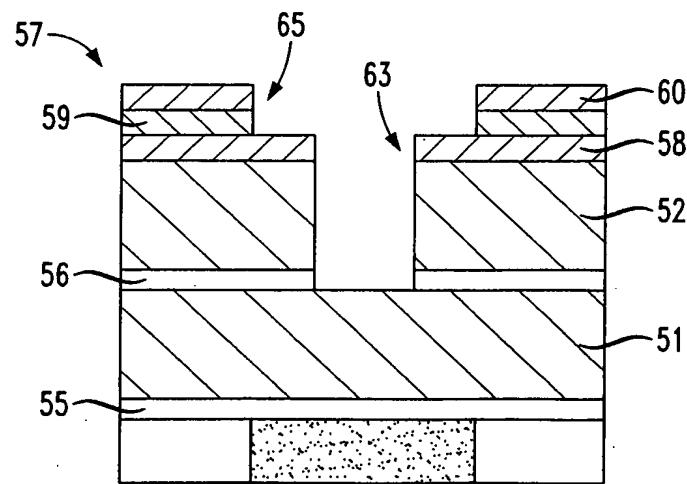


FIG. 22



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FIG. 23

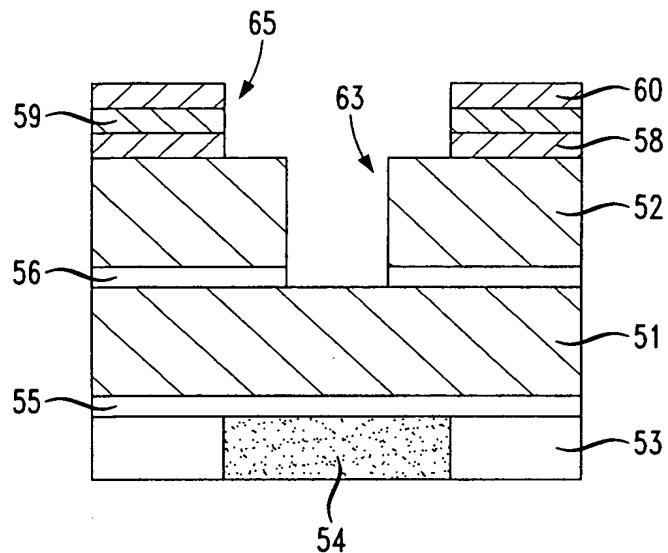
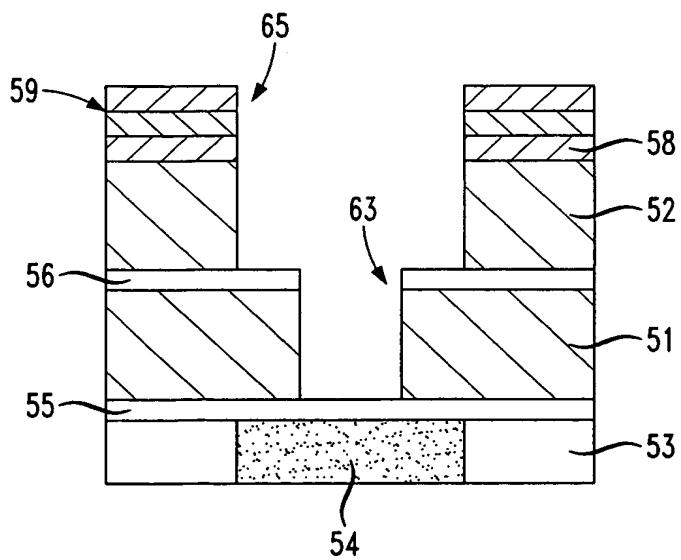


FIG. 24



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FIG. 25

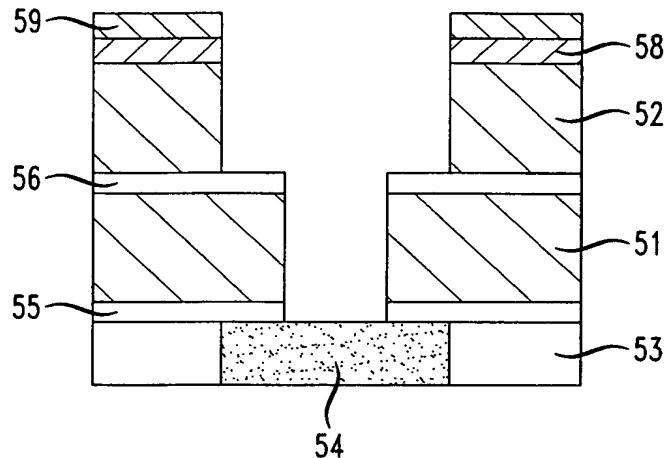
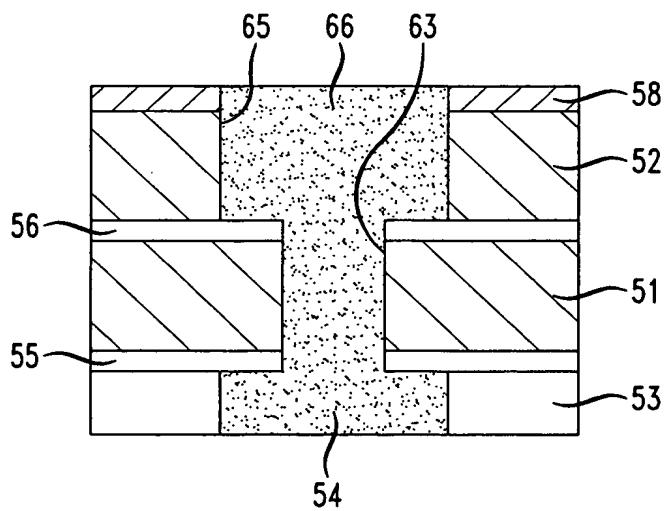


FIG. 26



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FIG. 27

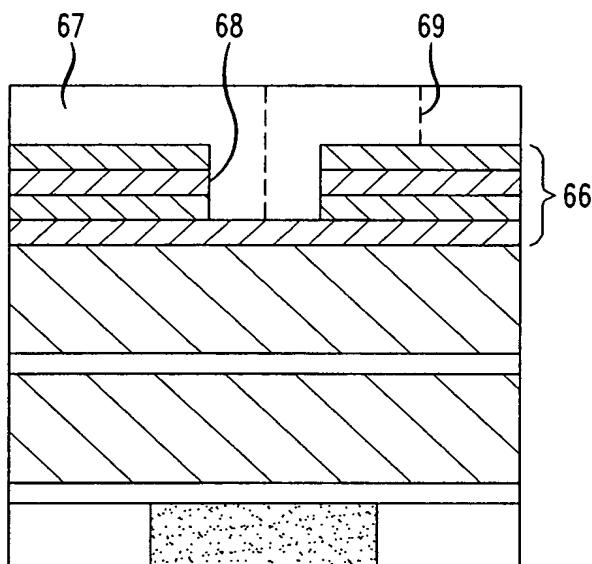
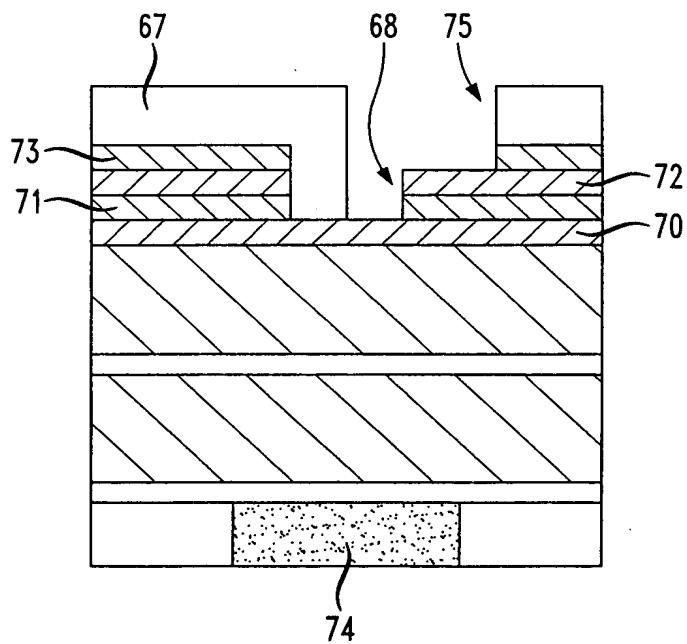


FIG. 28



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A Mask Layer and Interconnect Structure for Dual Damascene Fabrication of a Semiconductor Device  
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FIG. 29

